

TSMC-02-1050

October 15, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/619,114 07/14/03

Yi-Ming Sheu et al.

NARROW WIDTH EFFECT IMPROVEMENT
WITH PHOTORESIST PLUG PROCESS AND
STI CORNER ION IMPLANTATION

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on October 20, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

Stephen B. Ackerman 10/20/03

TSMC-02-1050

U.S. Patent 6,162,679 to Lin, "Method of Manufacturing DRAM Capacitor," discloses a method of forming trench type DRAM capacitor.

U.S. Patent 5,960,276 to Liaw et al., "Using an Extra Boron Implant to Improve the NMOS Reverse Narrow Width Effect in Shallow Trench Isolation Process," describes a method to reduce the reverse narrow width effect.

U.S. Patent 6,228,726 to Liaw, "Method to Suppress CMOS Device Latchup and Improve Interwell Isolation," discloses a boron implant used to dope a region under an open trench to improve latchup immunity and to increase the N+ to N well and P+ to P well isolation.

U.S. Patent 5,296,392 to Grula et al., "Method of Forming Trench Isolated Regions with Sidewall Doping," discusses a CVD process with dichlorosilane as the silicon source gas and diborane as the source of the boron dopant.


U.S. Patent 6,277,697 to Lee, "Method to Reduce Inverse-Narrow-Width Effect," discusses a tilted boron implant performed through a pad oxide into a substrate.

U.S. Patent 6,245,639 to Tsai et al., "Method to Reduce a Reverse Narrow Channel Effect for MOSFET Devices," discusses the RNCE being reduced by a large angle N ion implant into sidewalls of a trench which blocks B ions from migrating to an STI/well interface.

U.S. Patent 6,331,458 to Anjum et al., "Active Region Implant Methodology Using Indium to Enhance Short Channel Performance of a Surface Channel PMOS Device," describes a method for implanting indium ions in an active region between two field oxide regions formed by a LOCOS method.

U.S. Patent 6,504,219 to Puchner et al., "Indium Field Implant for Punchthrough Protection in Semiconductor Devices," discusses a technique for forming an indium field implant at the bottom of an STI trench to strengthen the p-well under field oxide, but to not weaken the n-well under the field oxide.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

Document Number (Sequence)

Applicant's Name

TSMC-02-1050

10/619, 114

Applicant

Yi-Ming Sheu et al.

Filing Date

07/14/03

Group Art Unit

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

(Use several sheets if necessary)

U. S. PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILED DATE & APPROPRIATE
	6162679	12/19/00	Lin	438	253	5/6/99
	5960276	9/28/99	Liaw et al.	438	224	9/28/98
	6228726	5/8/01	Liaw	438	294	3/6/00
	5296392	3/22/94	Grula et al.	437	34	2/24/92
	6277697	8/2/01	Lee	438	296	11/12/99
	6245639	6/12/01	Tsai et al.	438	424	2/8/99
	6331458	12/18/01	Anjum et al.	438	197	9/22/95
	6504219	1/7/03	Puchner et al.	257	371	9/24/01

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Portraits Pages, Etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.